REMARKS

This Amendment After Final Rejection is submitted in response to the outstanding final Office Action, dated January 29, 2004. Claims 1-4 and 7-15 are presently pending in the above-identified patent application. In this response, Applicants proposes to amend claims 1, 8, and 12. No additional fee is due.

This amendment is submitted pursuant to 37 CFR §1.116 and should be entered. The Amendment places all of the pending claims, i.e., claims 1-4 and 7-15, in a form that is believed allowable, and, in any event, in a better form for appeal.

The Examiner is thanked for the courtesy of a telephone interview on April 7, 2004. As discussed during the interview, independent claims 1, 8, and 12 have been amended based on the limitation of previously presented dependent claim 7. Thus, Applicants submit that no "new issues" are raised by the present amendment that would require a new search. It is thus believed that examination of the pending claims, as amended, which have been previously considered by the Examiner when examining claim 7, are consistent with the previous record herein and will not place any substantial burden on the Examiner. Applicants respectfully request entry of the amendment in the present application. No new matter is introduced.

In the Office Action, the Examiner rejected claims 1-4 and 7-15 under 35 U.S.C. §102(b) as being anticipated by Okazaki (United States Patent Number 5,214,330).

The present invention is directed to a bidirectional bus repeater that connects individual segments of a bidirectional bus. The exemplary bidirectional bus repeater consists of a direction control block and a buffer block. The buffer block contains one pair of buffers for each bus bit and an extra pair associated with the indicator lines. Indicator lines are used by the direction control block based on activity on the bus to generate control signals (control-A and control-B) that control the state of the tri-state buffers. In an exemplary embodiment, each node must toggle the indicator line whenever the node drives the bus. When the bus is inactive, the control-A and control-B signals generated by the direction control block are both inactive because the voltages on both sides of the bidirectional bus repeater are the same.

Independent Claims 1, 8 and 12

Independent claims 1, 8, and 12 were rejected under 35 U.S.C. §102(b) as being anticipated by Okazaki.

In the Response to Arguments section of the final Office Action, the Examiner asserts that Okazaki discloses a pair of indicator signals (S2 and S3), wherein a single voltage change (low (L) or high (H)) on one of the indicator signals (S2 and S3) causes one or more of the pair of buffers (11 and 12) to transfer data in a given direction for a finite period of time.

Applicants note that Okazaki teaches that buffer 12 will remain inactive and buffer 11 will remain active for as long as signal A is active. (See FIGS. 1 and 2; col. 3, lines 12-25.) Essentially, the assertion of SIGNAL A will generate a low level on the output of buffer 2. The low level output of S2 will disable buffer 3, thereby keeping the output of buffer 3 at a high level, thereby keeping buffer 2 and buffer 11 enabled. The low level output of S2 will also disable buffer 12. The signals on BUS A will then be able to propagate through buffer 11 to BUS B. Even when the propagation of the data from BUS A to BUS B is complete, buffer 11 will continue to transfer data from BUS A to BUS B until SIGNAL A is deasserted. Thus, Okazaki teaches that buffer 11 will transfer data in a given direction for a period of time based on the duration of SIGNAL A. Independent claims 1, 8, and 12, as amended, require a pair of indicator signals, wherein a single voltage change on one of said indicator signals causes each of said pair of buffers to transfer data in a given direction *for a finite period of time based on a time required for the second of said bus segments to reach the same logic level as the first of said bus segments*. It should also be noted that the word "finite" is defined by Dictionary.com as existing, persisting or enduring for a limited time only.

Thus, Okazaki does not disclose or suggest a pair of indicator signals, wherein a single voltage change on one of said indicator signals causes each of said pair of buffers to transfer data in a given direction for a finite period of time based on a time required for the second of said bus segments to reach the same logic level as the first of said bus segments, as required by independent claims 1, 8, and 12, as amended.

<u>Dependent Claims 2-4, 7, 9-11 and 13-15</u>

Dependent claims 2-4, 7, 9-11 and 13-15 were rejected under 35 U.S.C. §102(b) as being anticipated by Okazaki.

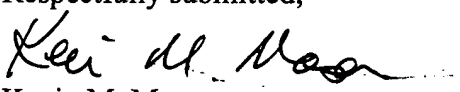
Claims 2-4 and 7, 9-11 and 13-15 are dependent on claims 1, 8, and 12, respectively, and are therefore patentably distinguished over Okazaki because of their dependency from amended independent claims 1, 8, and 12 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims, i.e., claims 1-4 and 7-15, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,



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